SEGMENTED DATALINE SCHEME IN A MEMORY WITH ENHANCED FULL FAULT COVERAGE MEMORY CELL TESTABILITY

ABSTRACT

A memory includes a plurality of row segments, with each row segment having a number of memory cells coupled to a corresponding dataline segment pair. Dataline driver circuits are provided between row segments to buffer signals on adjacent dataline segments. A control circuit is coupled to at least one row segment, and provides control signals to the at least one row segment and to the dataline driver circuits.